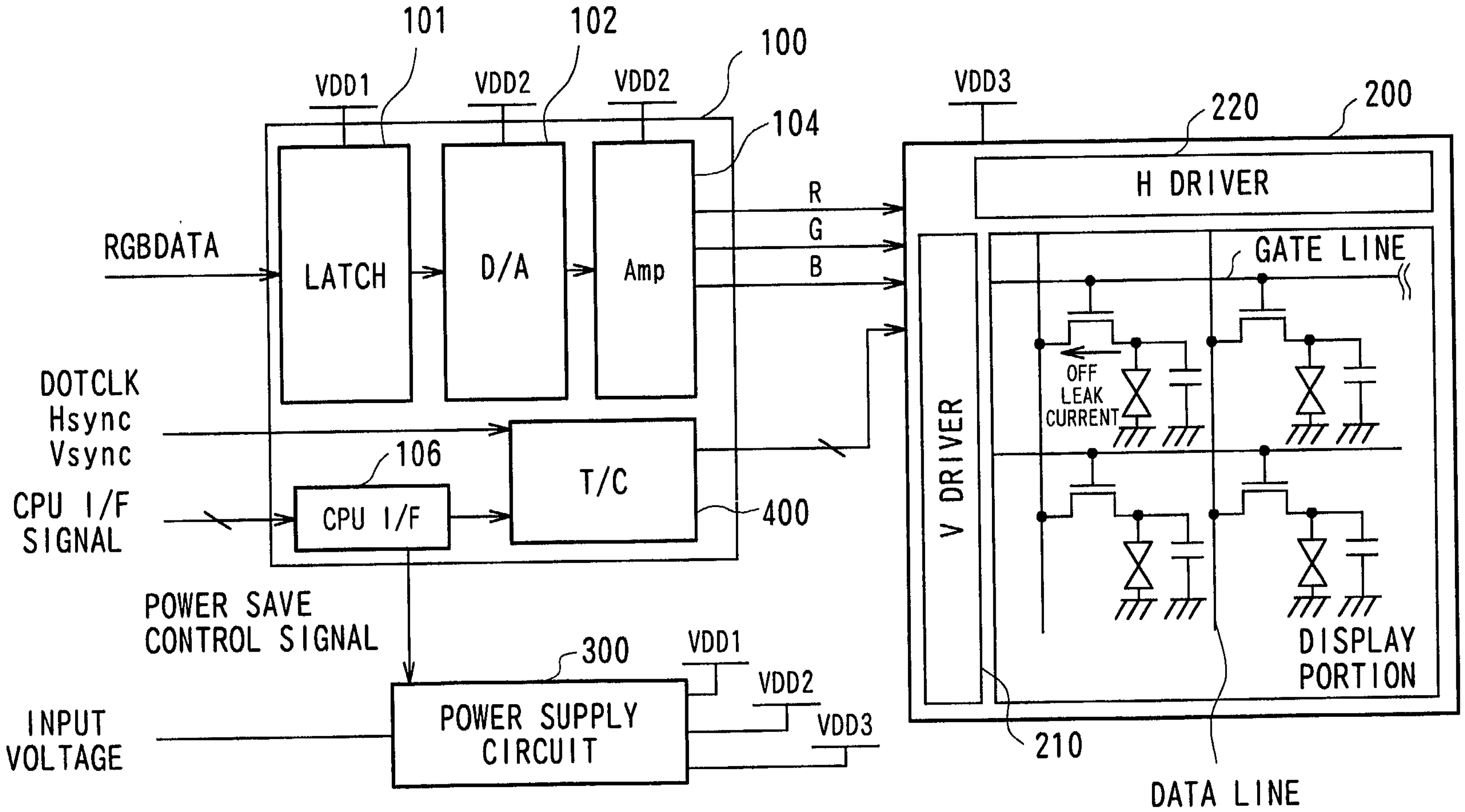

101
102
100
VDD1
VDD2
VDD2
104
VDD3
220
200
H DRIVER
RGBDATA
LATCH
D/A
Amp
R
G
B
GATE LINE
DOTCLK
Hsync
Vsync
OFF
LEAK
CURRENT
V DRIVER
106
T/C
CPU I/F
SIGNAL
CPU I/F
400
POWER SAVE
CONTROL SIGNAL
300
VDD1
VDD2
VDD3
DISPLAY
PORTION
INPUT
VOLTAGE
POWER SUPPLY
CIRCUIT
210
DATA LINE

FIG. 1

FIG. 2 (a)

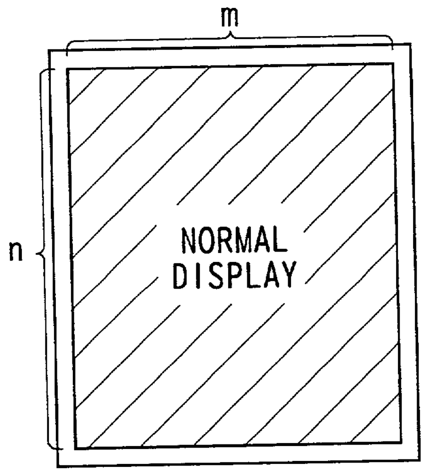


FIG. 2 (b)

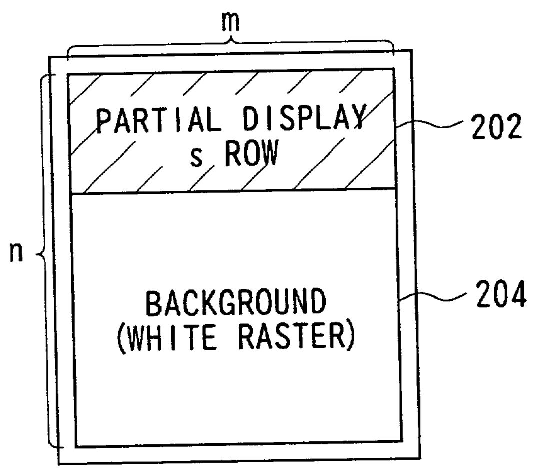
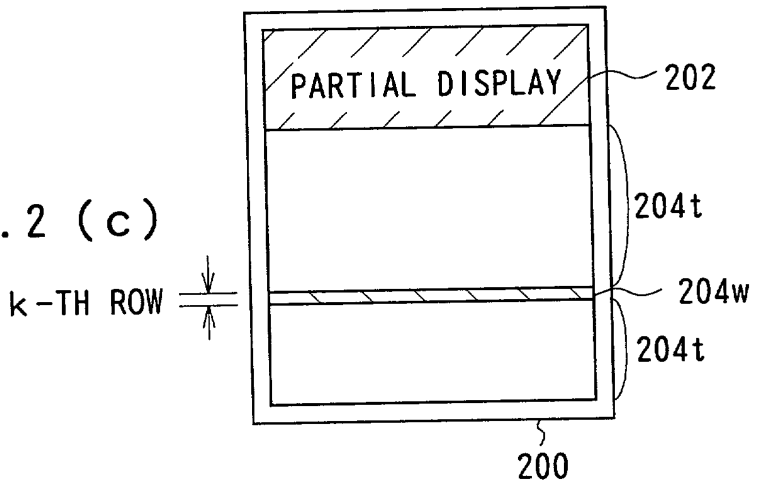


FIG. 2 (c)



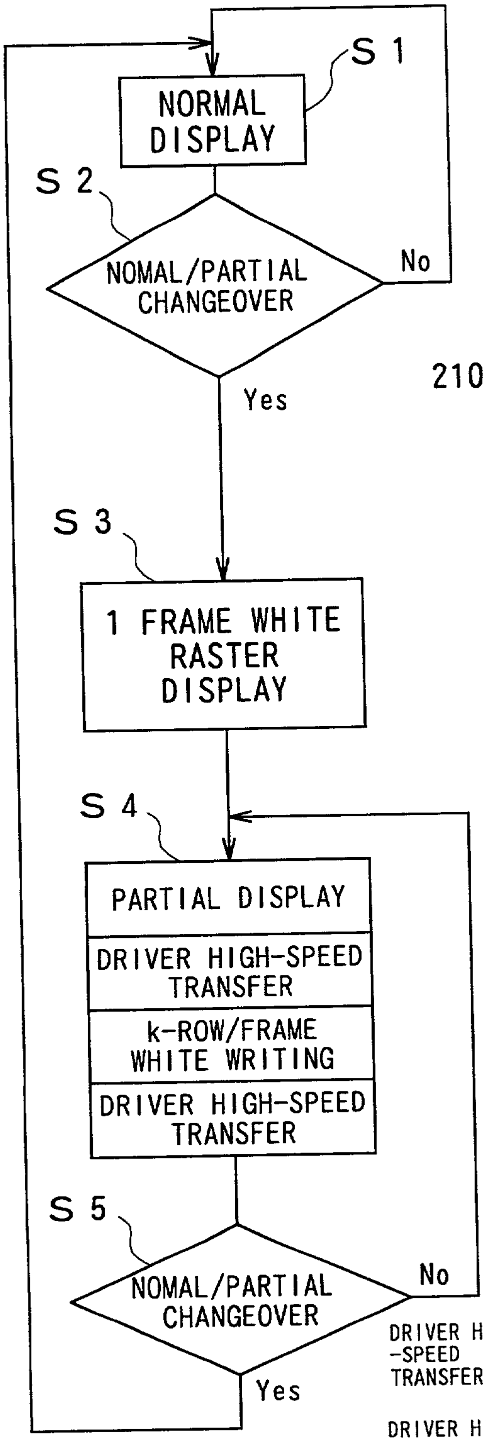


FIG. 3 (d)

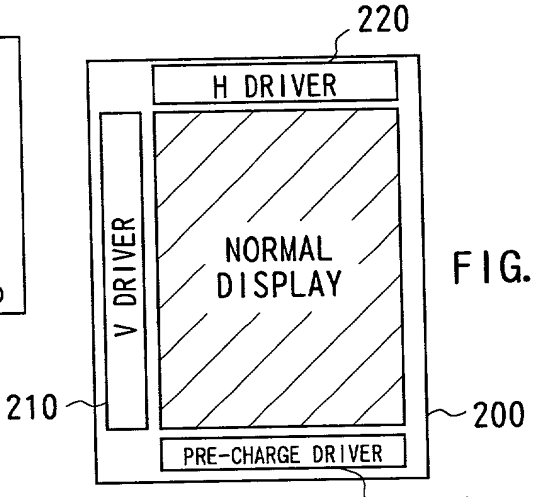


FIG. 3 (a)

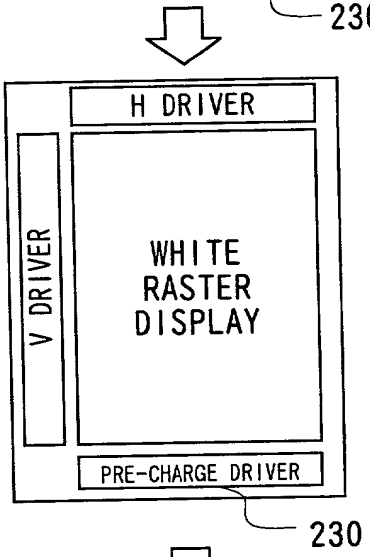


FIG. 3 (b)

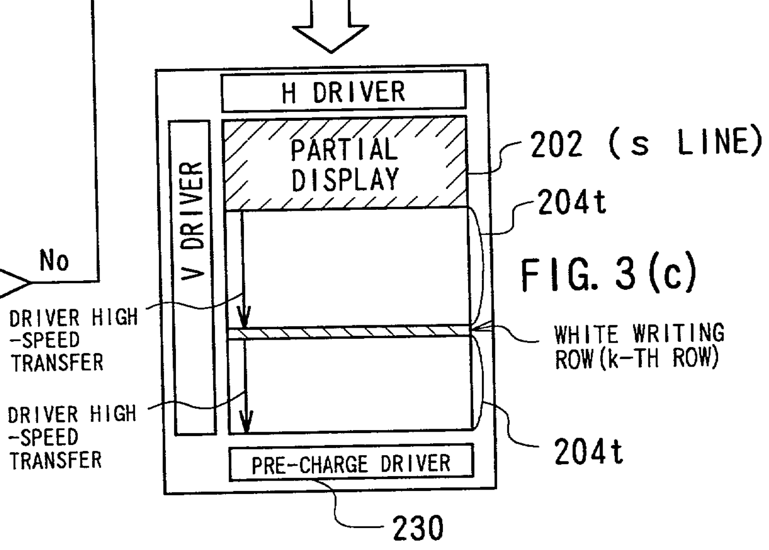


FIG. 3 (c)

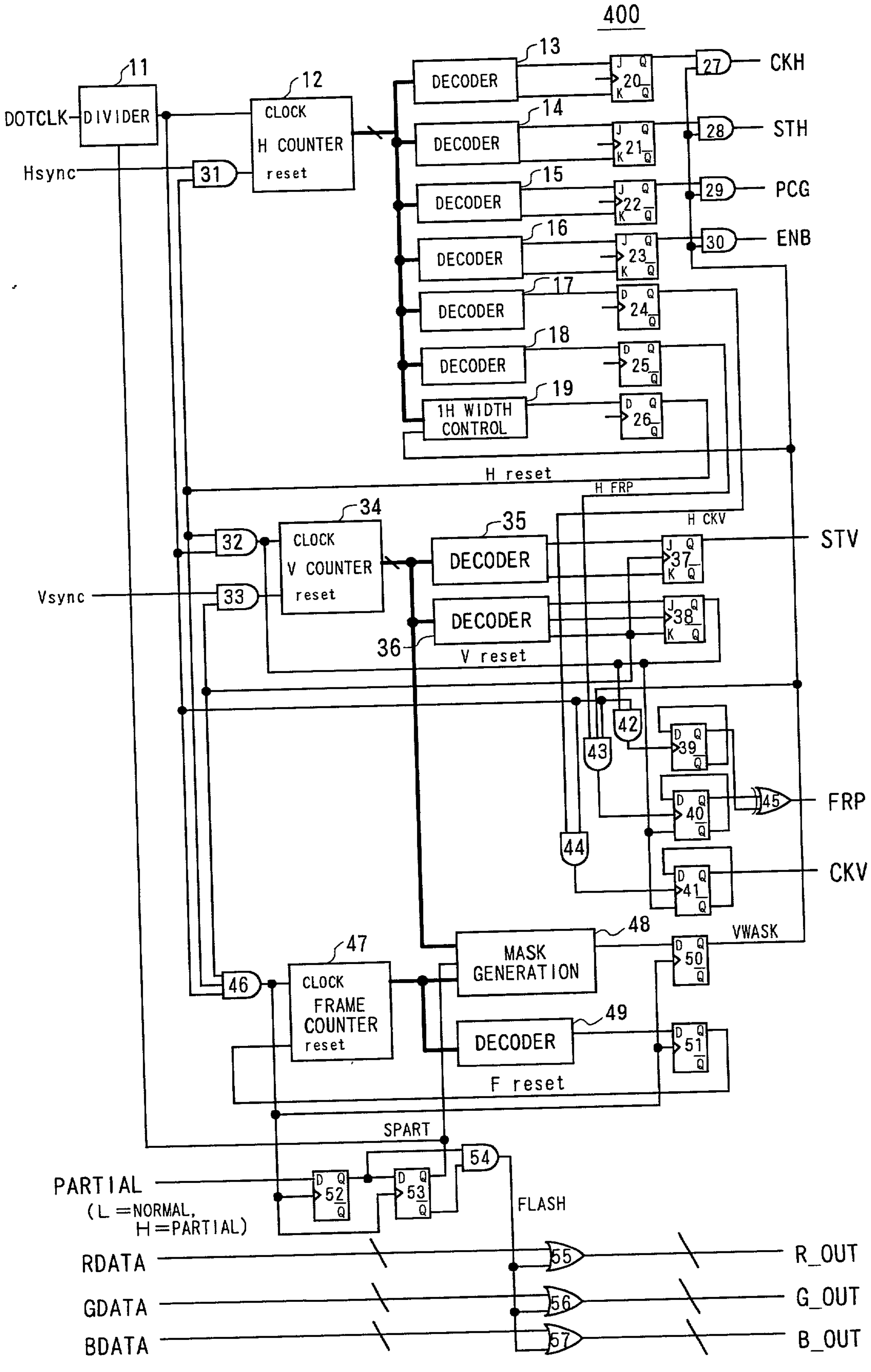

400
11
DOTCLK
DIVIDER
12
CLOCK
H COUNTER
reset
Hsync
31
13
14
15
16
17
18
19
DECODER
DECODER
DECODER
DECODER
DECODER
DECODER
1H WIDTH CONTROL
20
21
22
23
24
25
26
27
28
29
30
CKH
STH
PCG
ENB
H reset
H FRP
H CKV
32
33
34
CLOCK
V COUNTER
reset
Vsync
35
DECODER
DECODER
36
V reset
37
38
STV
39
40
41
42
43
44
45
FRP
CKV
46
47
CLOCK
FRAME COUNTER
reset
48
MASK GENERATION
49
DECODER
50
51
VWASK
F reset
SPART
52
53
54
PARTIAL
(L =NORMAL,
H =PARTIAL)
FLASH
RDATA
GDATA
BDATA
55
56
57
R_OUT
G_OUT
B_OUT

FIG. 4

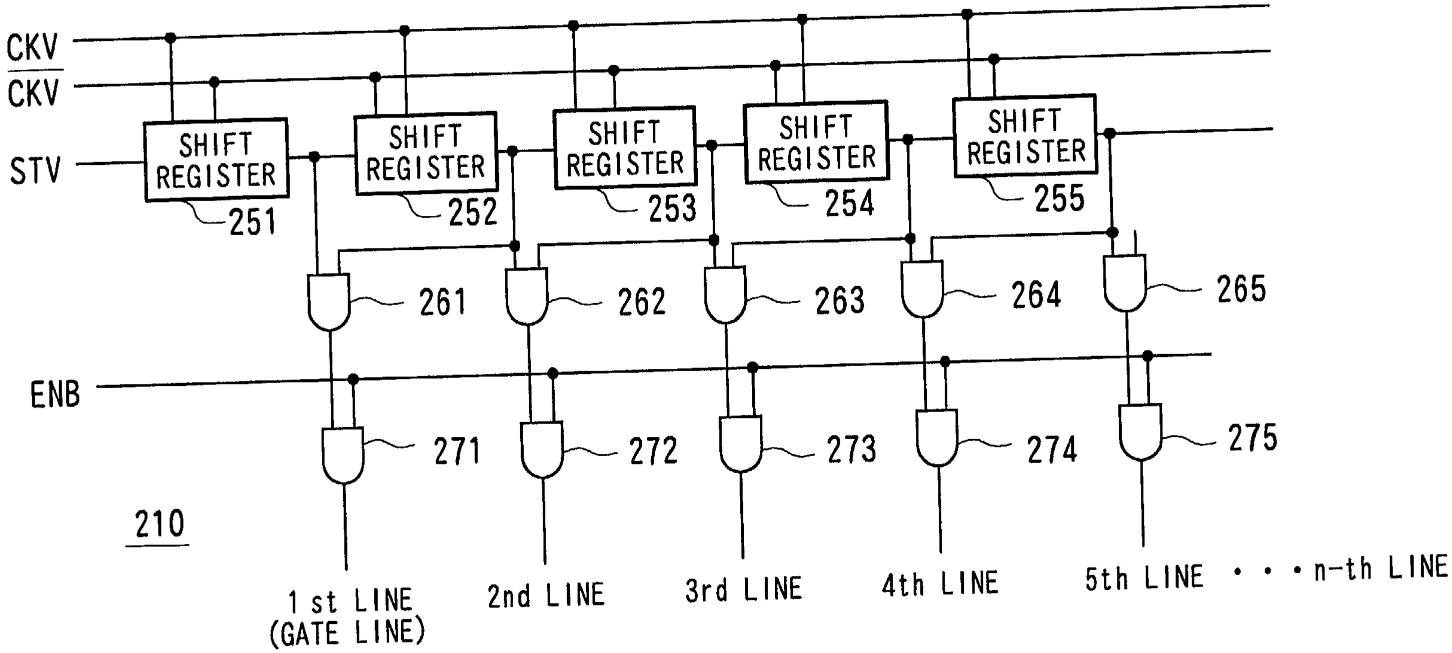

CKV
$\overline{\text{CKV}}$
STV
ENB
SHIFT REGISTER
251
SHIFT REGISTER
252
SHIFT REGISTER
253
SHIFT REGISTER
254
SHIFT REGISTER
255
261
262
263
264
265
271
272
273
274
275
210
1 st LINE (GATE LINE)
2nd LINE
3rd LINE
4th LINE
5th LINE • • • n-th LINE

FIG. 5

11:FREQUENCY DIVIDER(DIVIDE-BY-FOUR CIRCUIT)

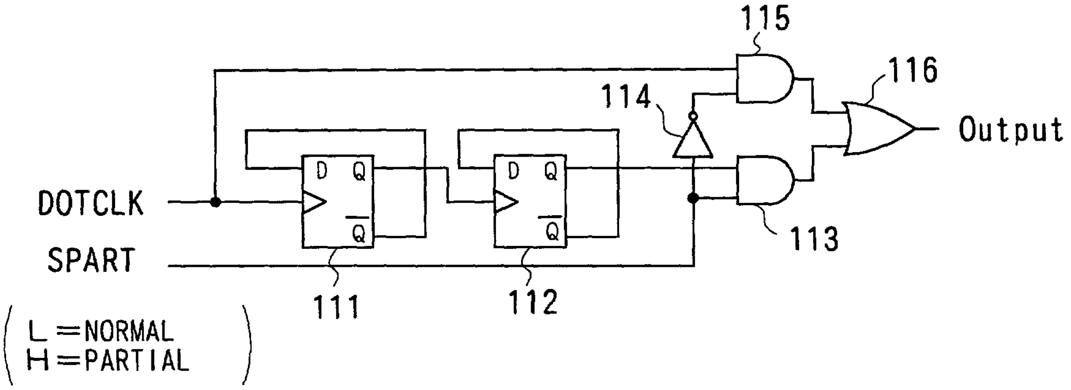
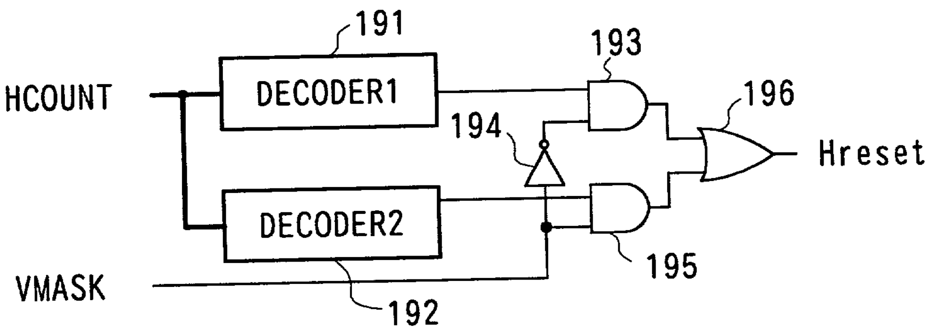


FIG. 6

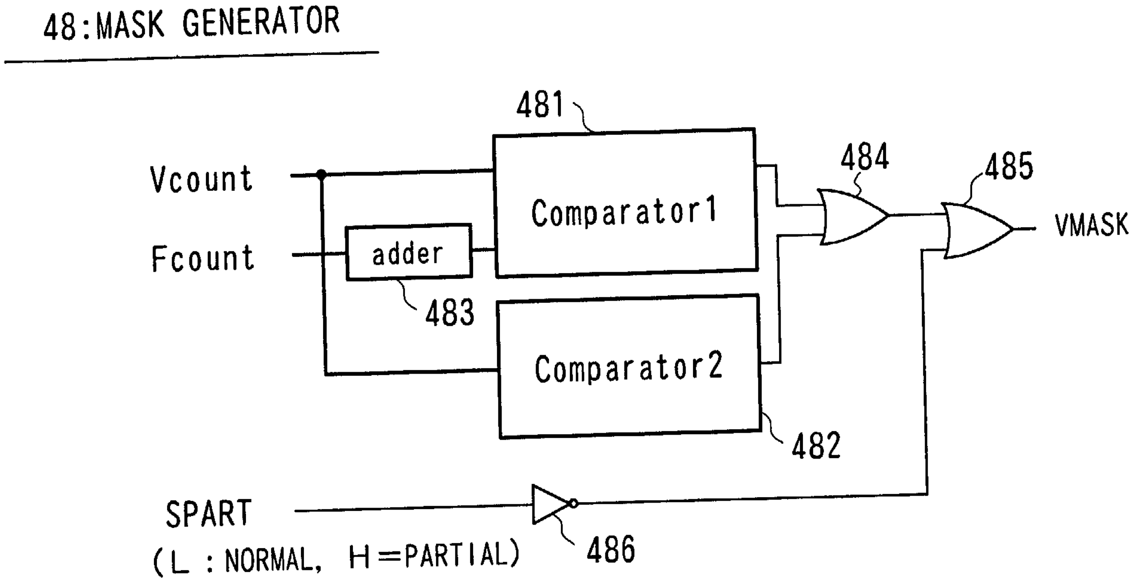
19:1H WIDTH CONTROL CIRCUIT



DECODER1 : if (COUNT=10) →H
else →L
DECODER2 : if (COUNT=120) →H
else →L

FIG. 7

48:MASK GENERATOR



Comparator1 : if (Vcount=Fcount+25) →H
else →L
Comparator2 : if (Vcount<25) →H
else →L

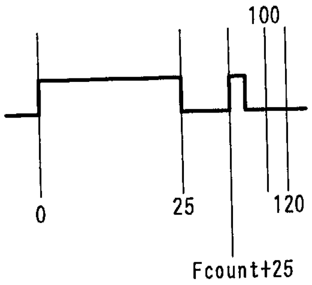
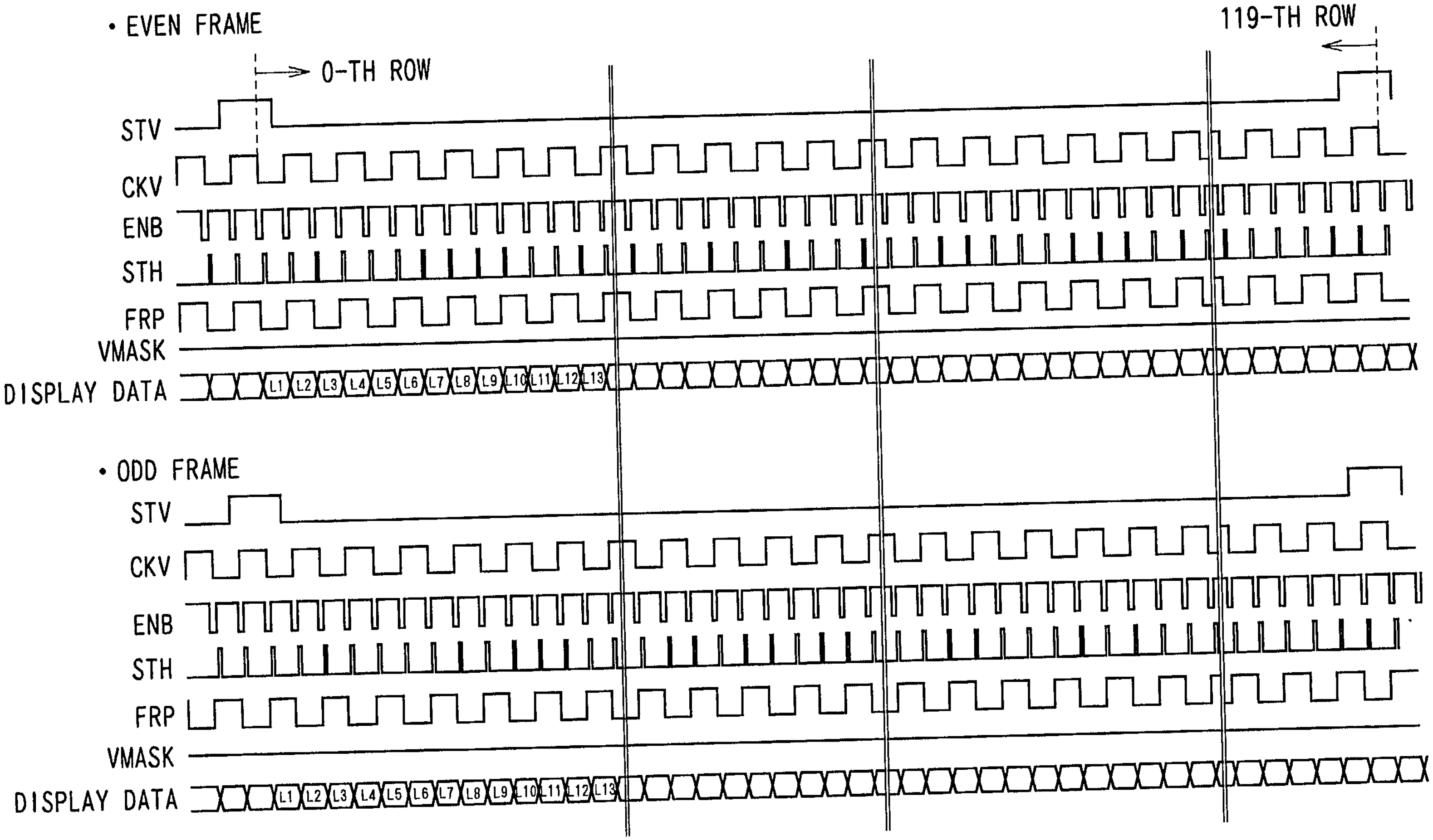
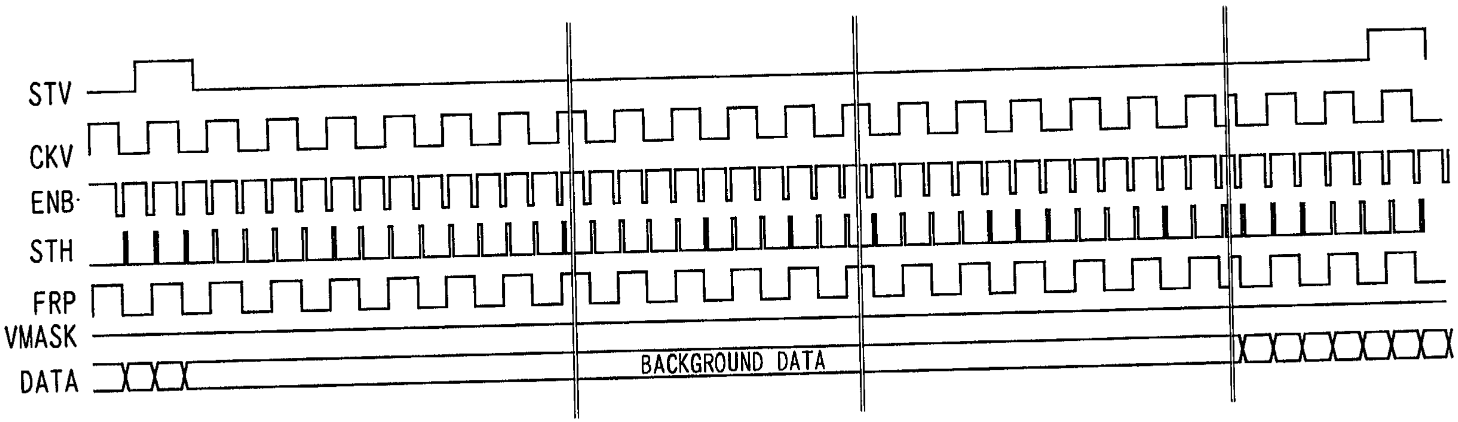


FIG. 8



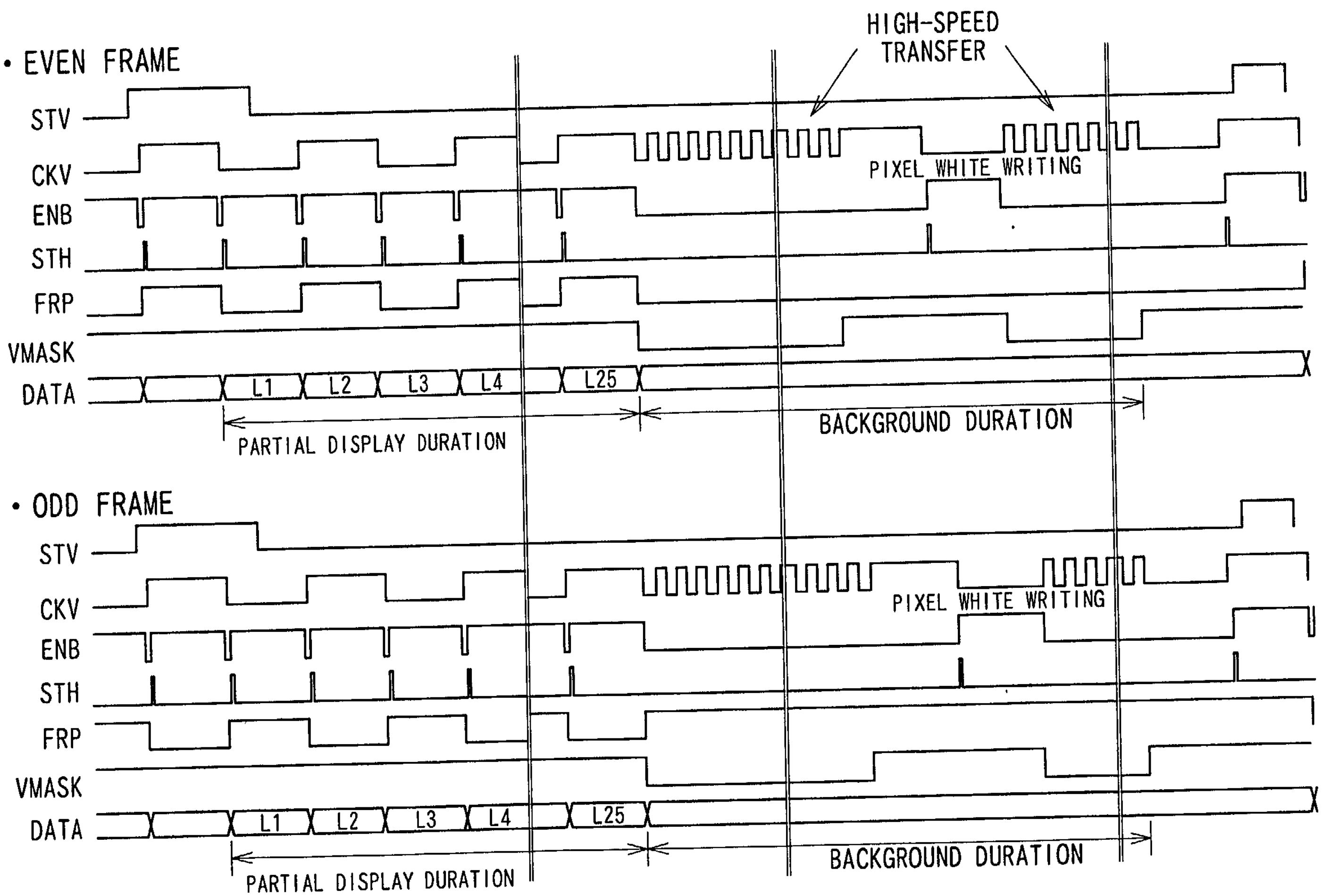
TIMING CHART IN NORMAL DISPLAY

FIG. 9



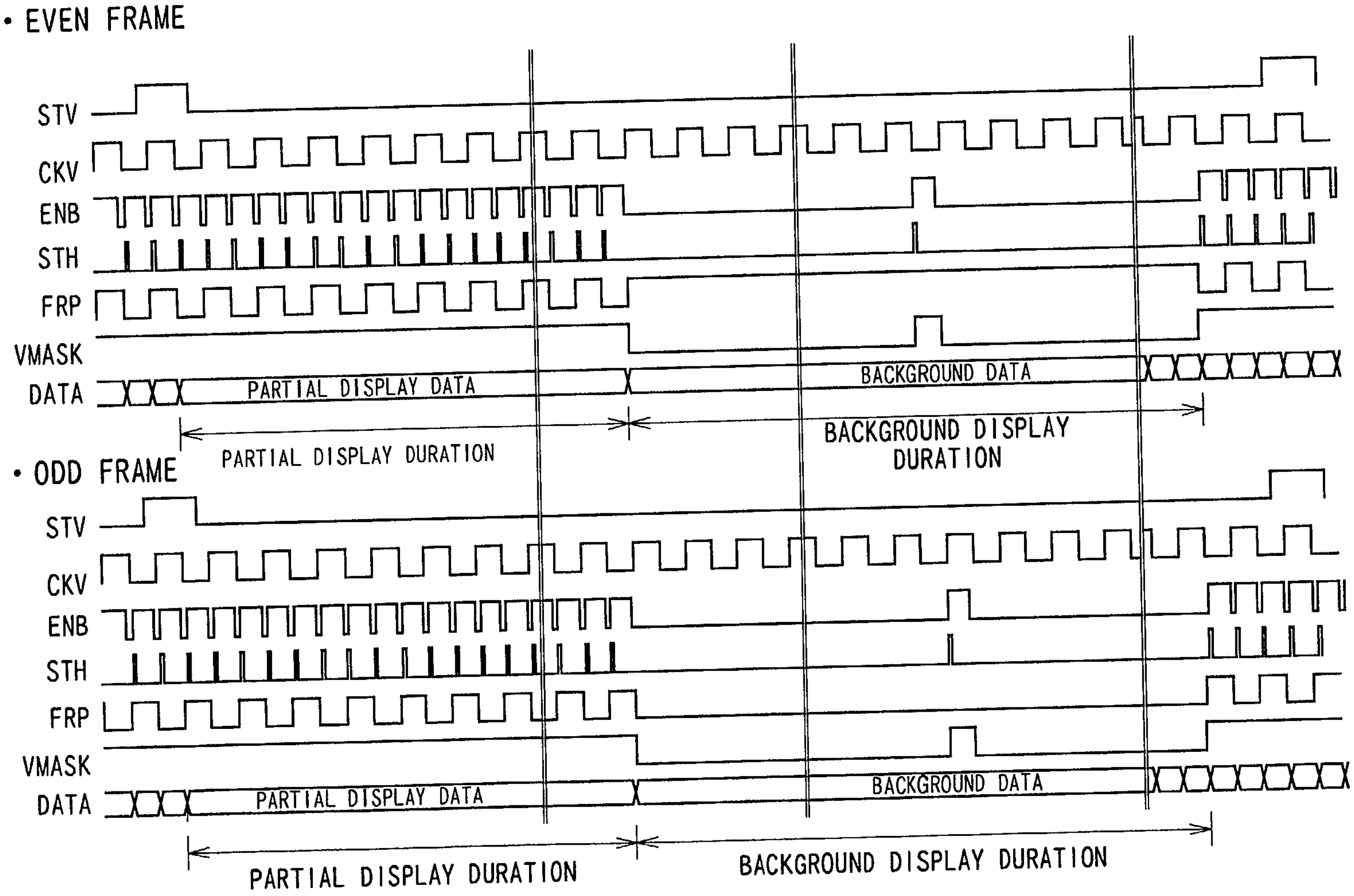
TIMING CHART IN BACKGROUND DISPLAY

FIG. 10



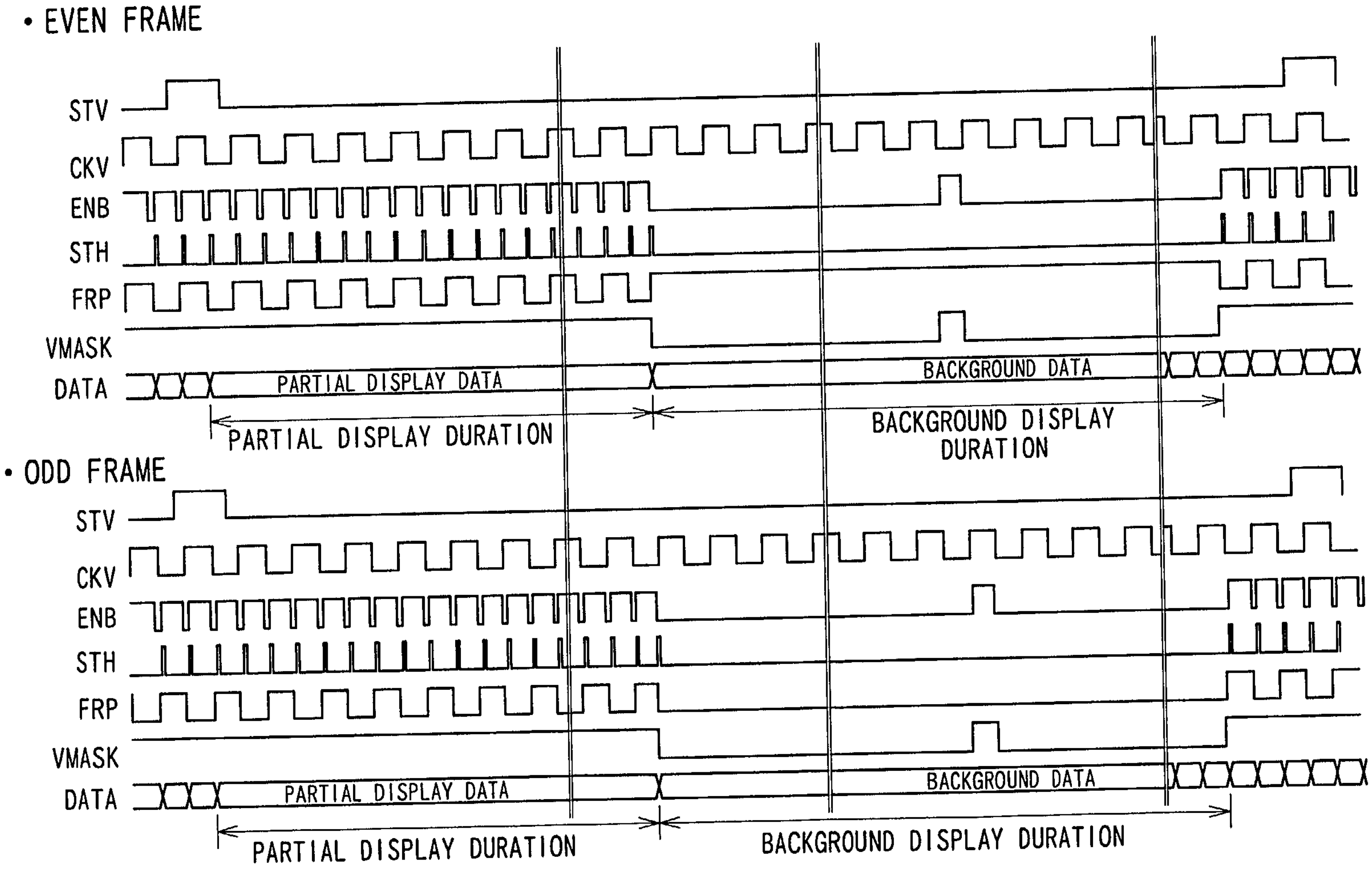
TIMING CHART IN PARTIAL DISPLAY (DRIVING METHODS 1 AND 4)

FIG. 11



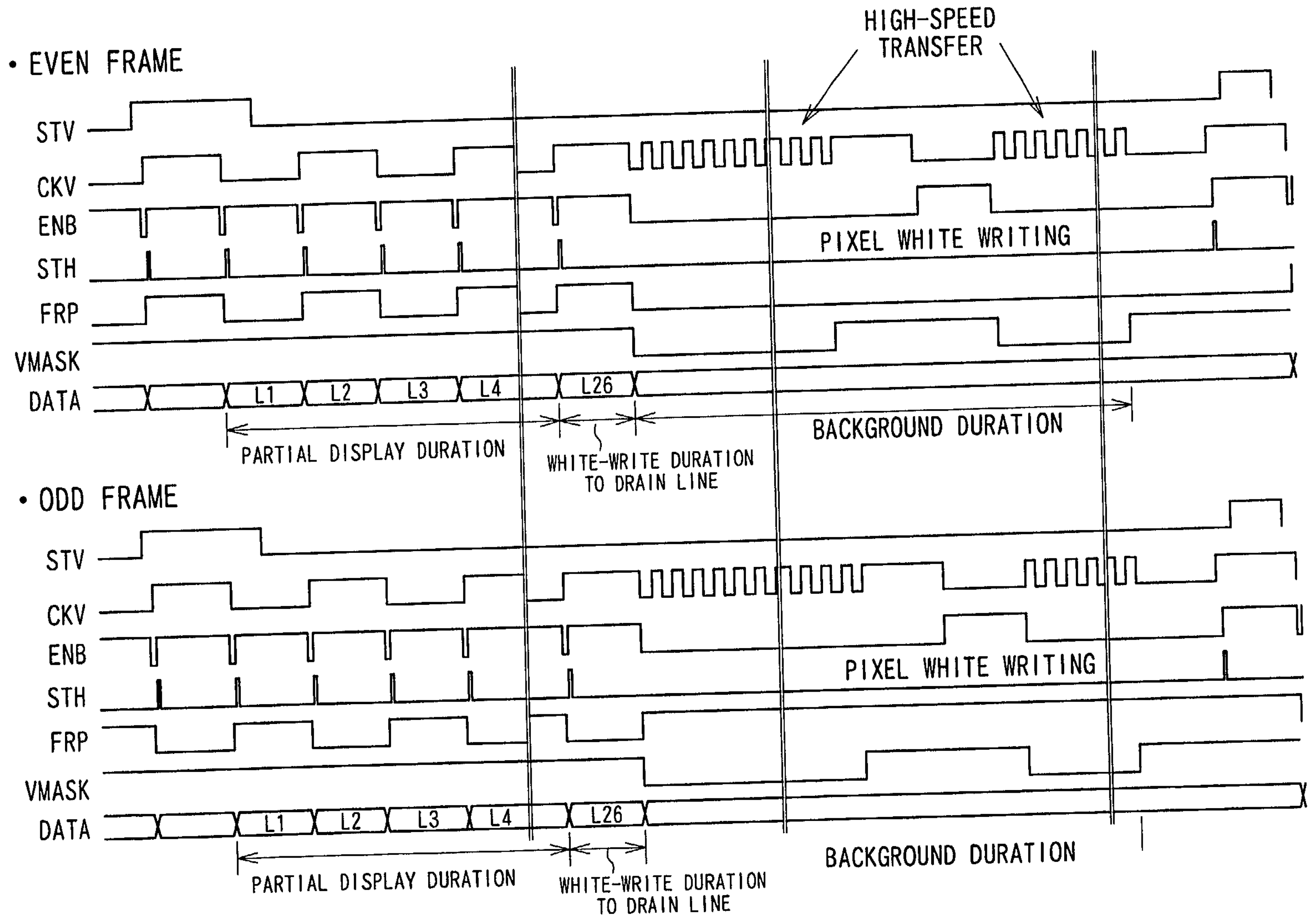
TIMING CHART IN PARTIAL DISPLAY (DRIVING METHOD 1)

FIG. 12



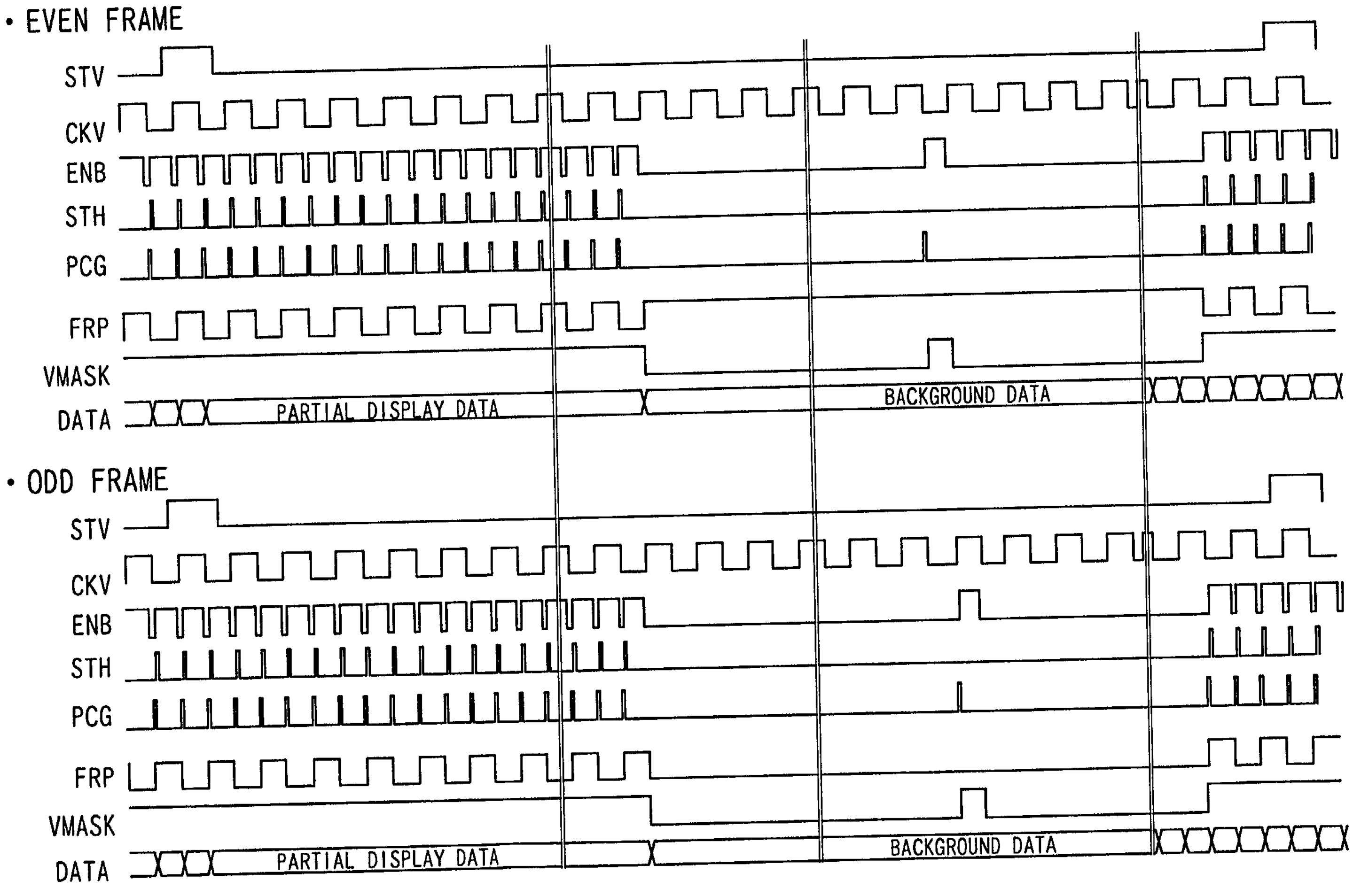
TIMING CHART IN PARTIAL DISPLAY (DRIVING METHOD 2)

FIG. 13



TIMING CHART IN PARTIAL DISPLAY (DRIVING METHODS 2 AND 4)

FIG. 14



TIMING CHART IN PARTIAL DISPLAY (DRIVING METHOD 3)

FIG. 15

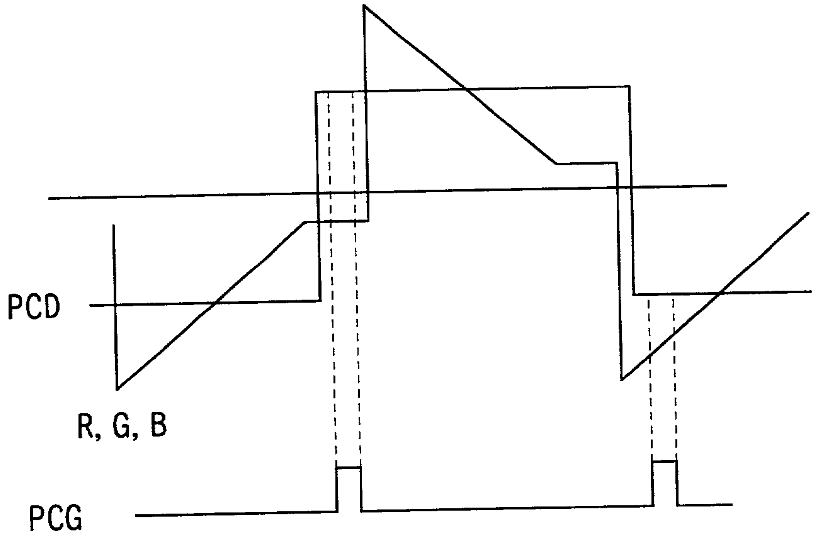
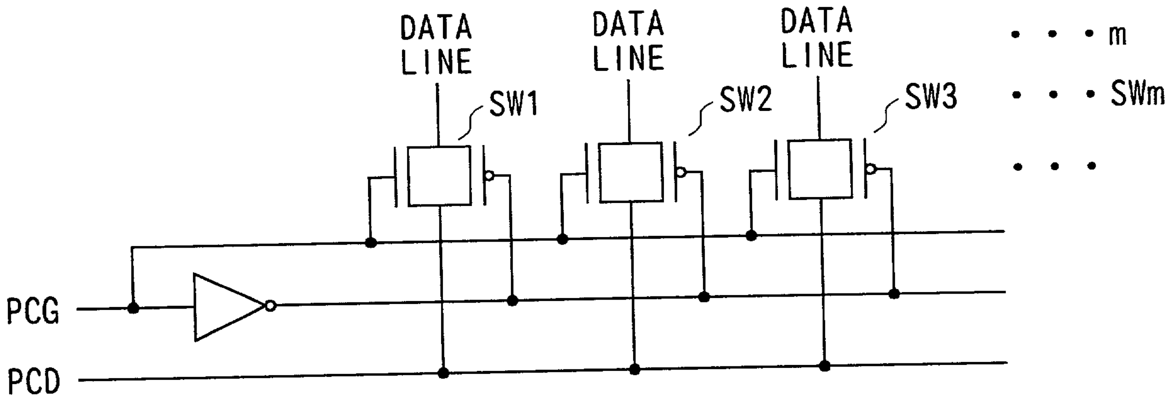
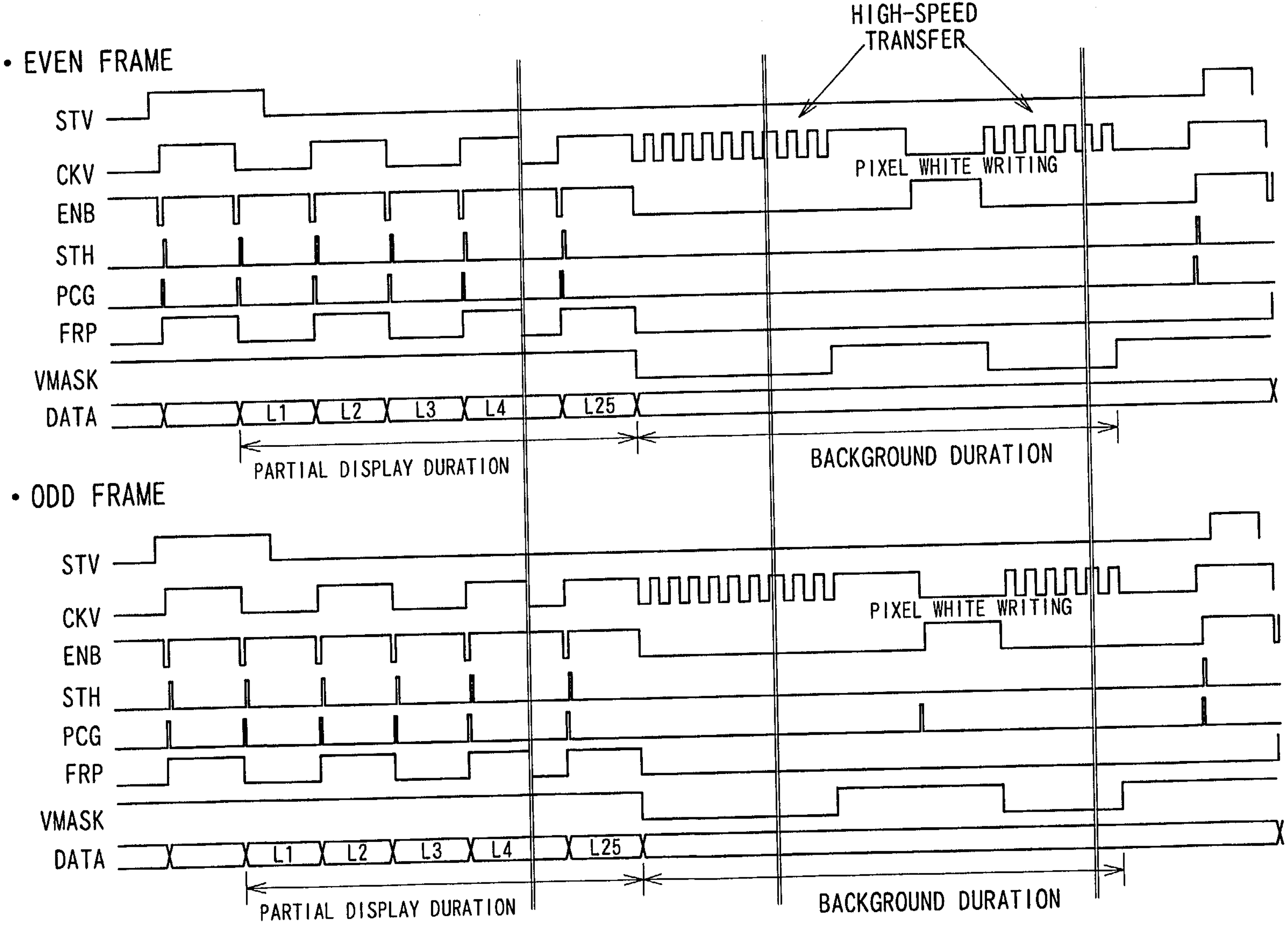


FIG. 16



230 : PRE-CHARGE DRIVER

FIG. 17



TIMING CHART IN PARTIAL DISPLAY (DRIVING METHODS 3 AND 4)

FIG. 18

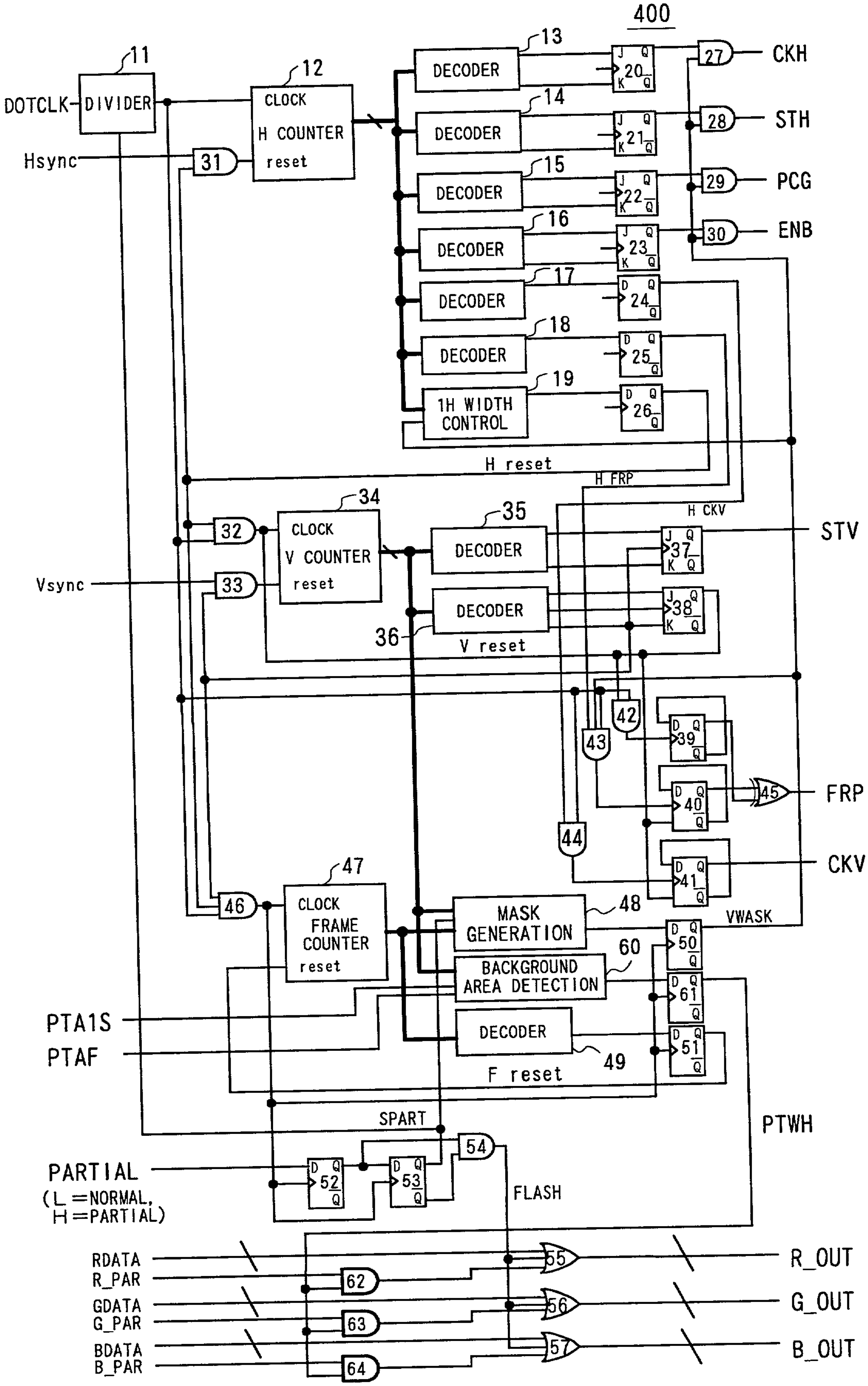
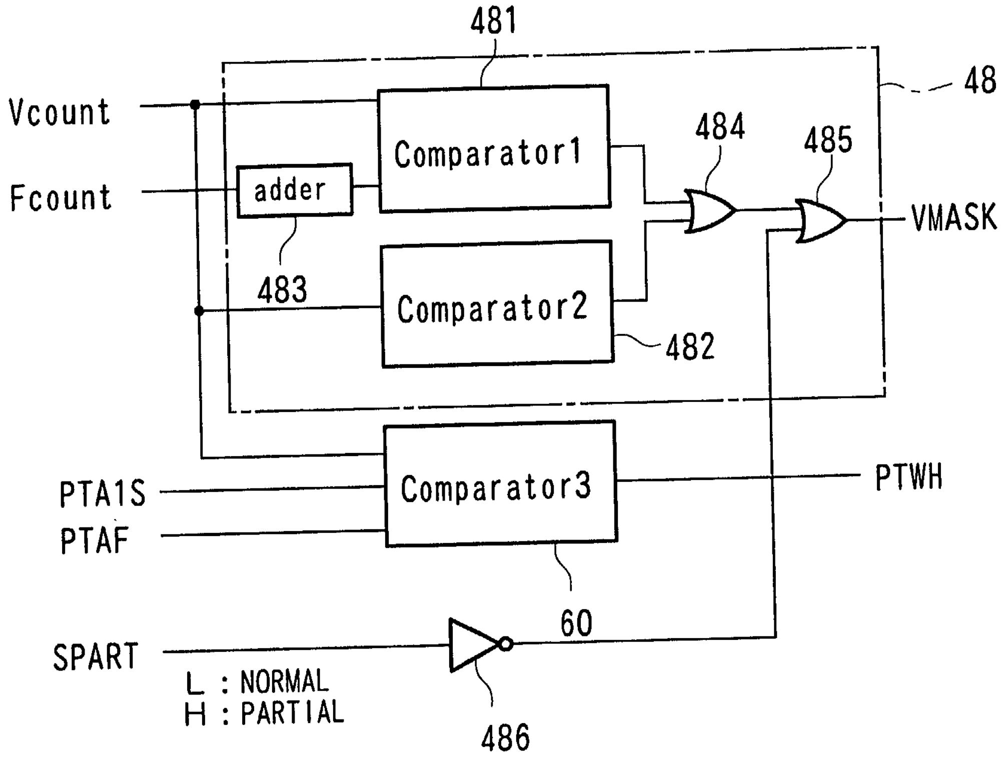
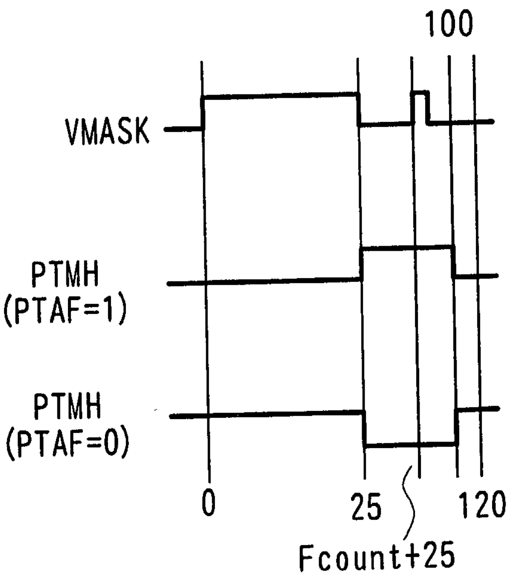

400
DOTCLK
DIVIDER
11
CLOCK
H COUNTER
reset
12
Hsync
31
DECODER
13
14
15
16
17
18
1H WIDTH CONTROL
19
J
K
Q
D
20
21
22
23
24
25
26
27
28
29
30
CKH
STH
PCG
ENB
H reset
H FRP
H CKV
32
33
CLOCK
V COUNTER
reset
34
35
36
Vsync
V reset
37
38
STV
42
43
44
39
40
41
45
FRP
CKV
46
CLOCK
FRAME COUNTER
reset
47
MASK GENERATION
48
VWASK
BACKGROUND AREA DETECTION
60
50
61
51
DECODER
49
F reset
PTA1S
PTAF
PTWH
SPART
54
52
53
PARTIAL
(L =NORMAL,
H =PARTIAL)
FLASH
RDATA
R_PAR
GDATA
G_PAR
BDATA
B_PAR
62
63
64
55
56
57
R_OUT
G_OUT
B_OUT

FIG. 19





```
Comparator3:if(PTAF=1)
             if(Vcount<25)      →Low
             else               →High
           elseif(Vcount<25)    →High
           else                 →Low
```

FIG. 20

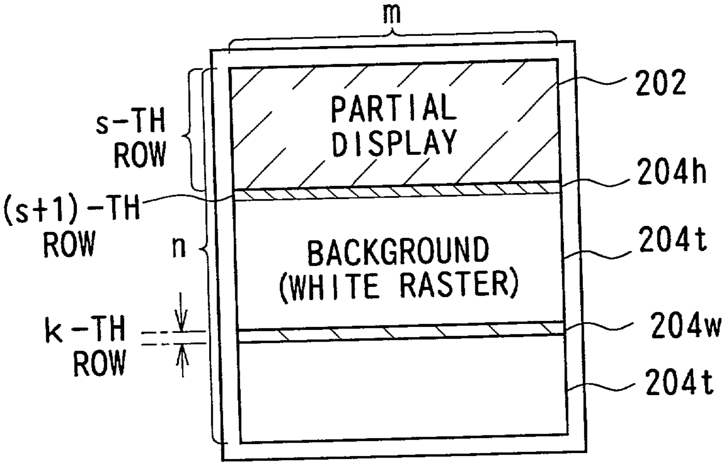

m
s-TH ROW
(s+1)-TH ROW
n
k-TH ROW
PARTIAL DISPLAY
BACKGROUND (WHITE RASTER)
202
204h
204t
204w
204t

FIG. 21

```
Comparator1:if(Vcount=fcount+25+1)→High
            else                  →Low


Comparator2:if(Vcount<25+1)→High
            else           →Low


Comparator3:if(PTAF=1)
              if(Vcount<25+1)  →Low
              else             →High
            elseif(Vcount<25)  →High
            else               →Low
```

FIG. 22

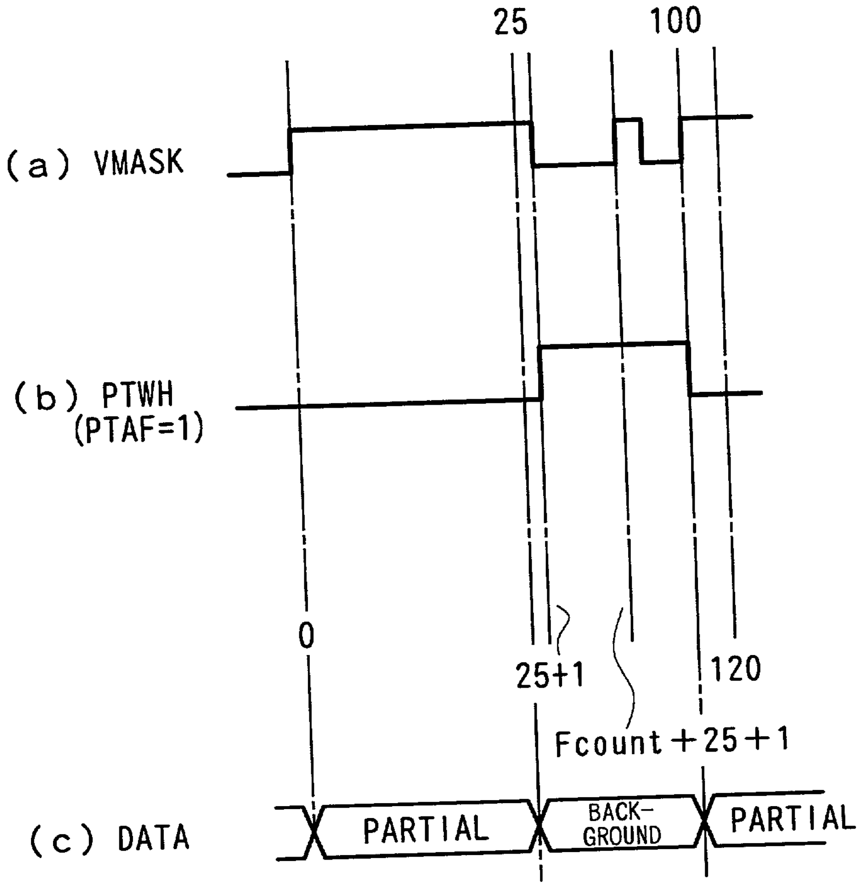

25
100
(a) VMASK
(b) PTWH
(PTAF=1)
0
25+1
120
Fcount＋25＋1
(c) DATA
PARTIAL
BACK-
GROUND
PARTIAL

FIG. 23

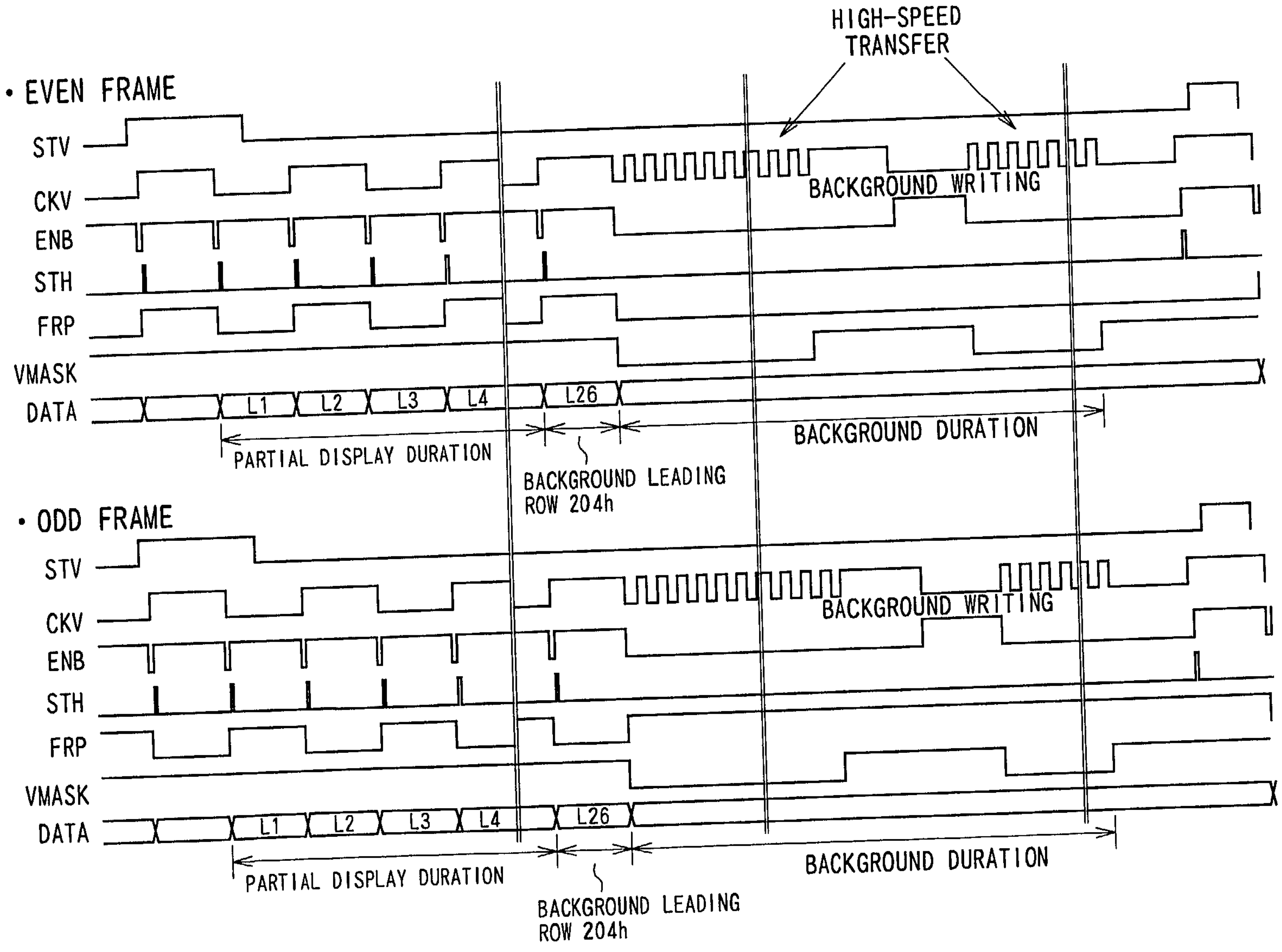

HIGH-SPEED TRANSFER
• EVEN FRAME
STV
CKV
ENB
STH
FRP
VMASK
DATA
L1
L2
L3
L4
L26
BACKGROUND WRITING
PARTIAL DISPLAY DURATION
BACKGROUND LEADING ROW 204h
BACKGROUND DURATION
• ODD FRAME
STV
CKV
ENB
STH
FRP
VMASK
DATA
L1
L2
L3
L4
L26
BACKGROUND WRITING
PARTIAL DISPLAY DURATION
BACKGROUND LEADING ROW 204h
BACKGROUND DURATION

FIG. 24

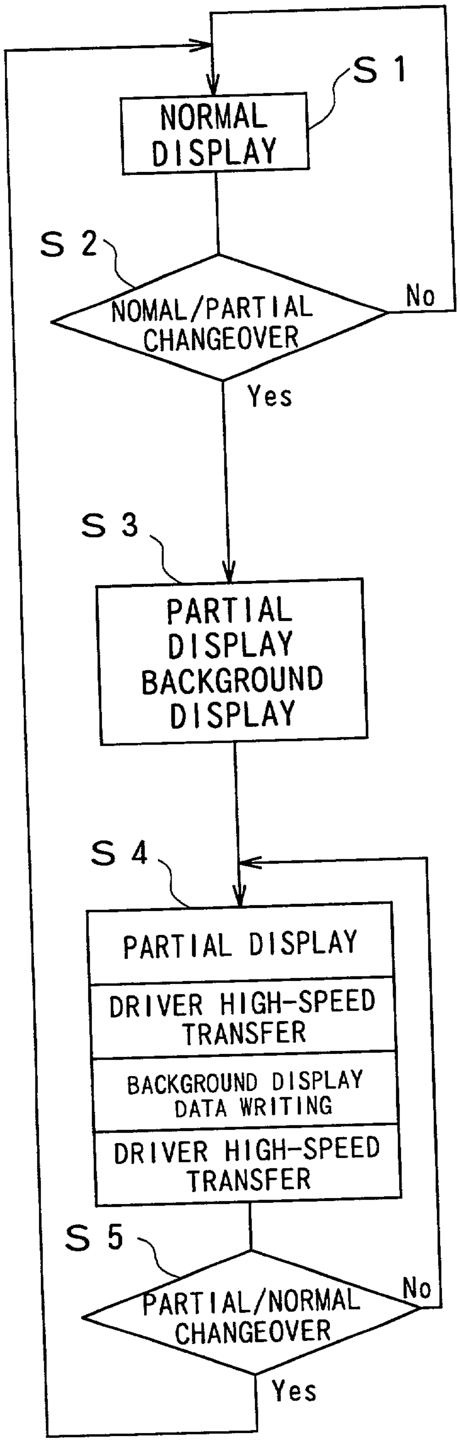


FIG. 25 (d)

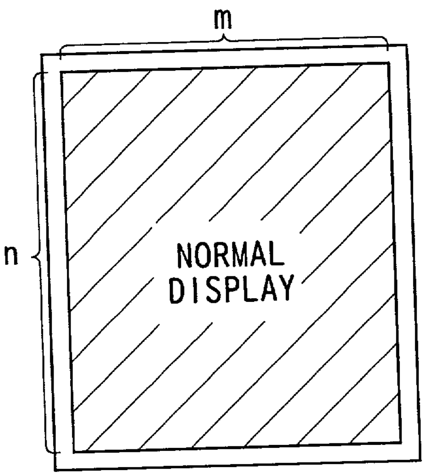


FIG. 25 (a)

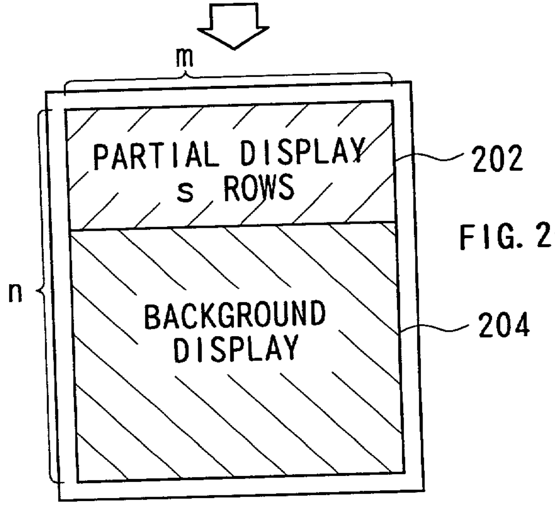


FIG. 25 (b)

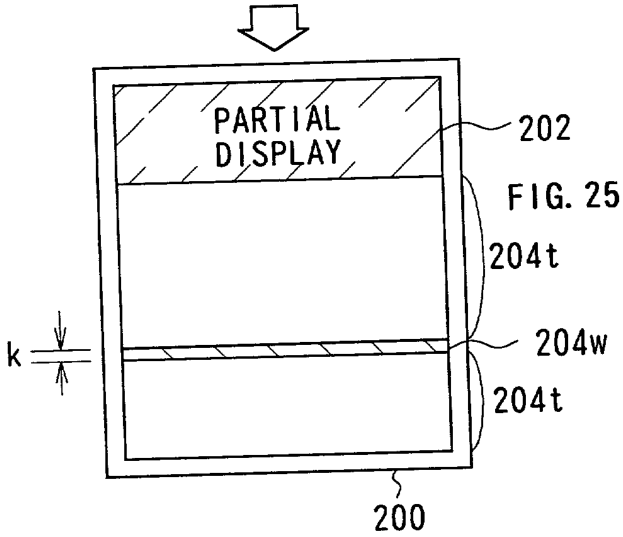
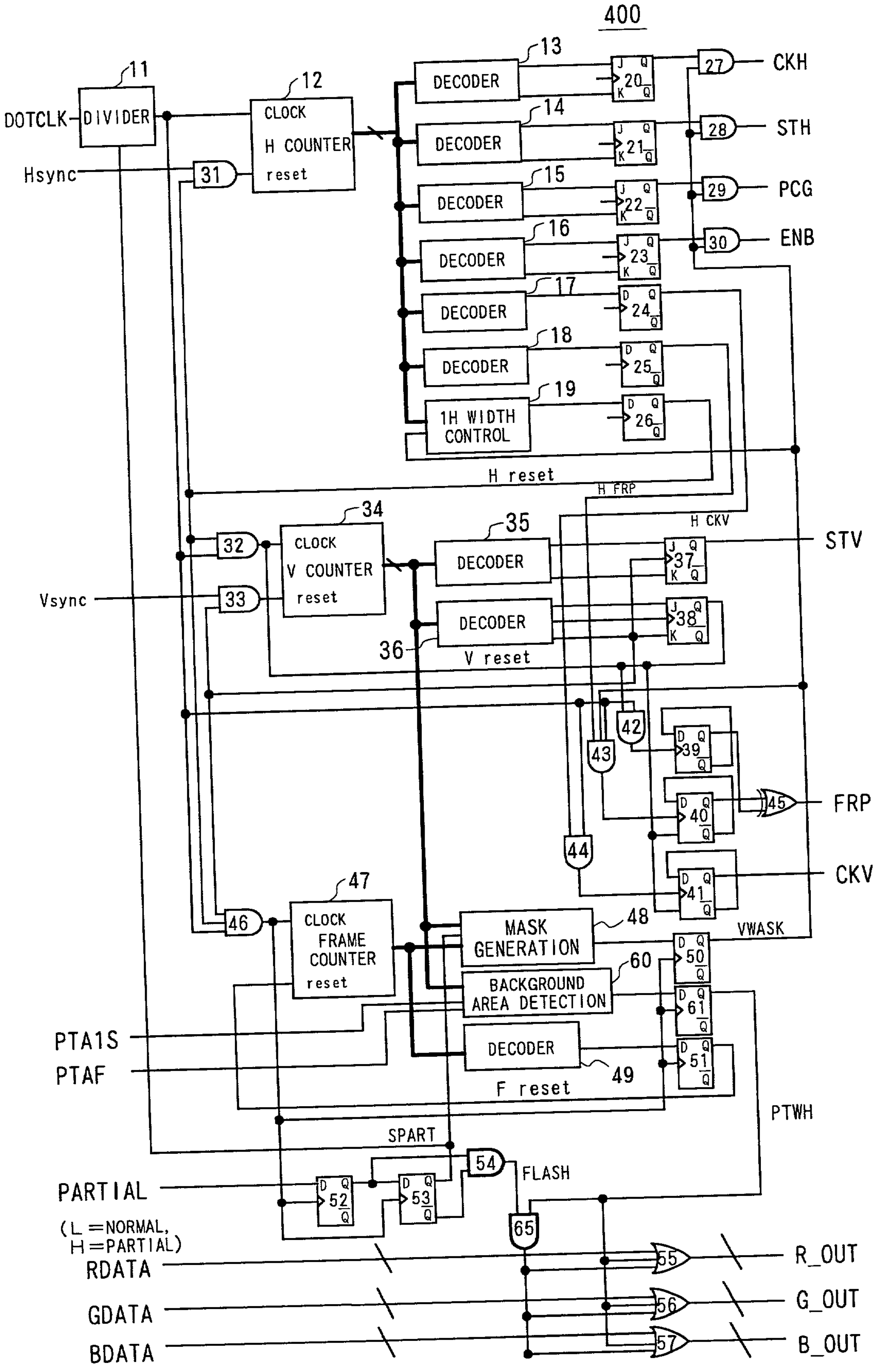


FIG. 25 (c)



400
DOTCLK
DIVIDER
11
Hsync
31
CLOCK
H COUNTER
reset
12
DECODER
13
14
15
16
17
18
1H WIDTH CONTROL
19
20
21
22
23
24
25
26
27
28
29
30
CKH
STH
PCG
ENB
H reset
H FRP
H CKV
32
33
Vsync
CLOCK
V COUNTER
reset
34
DECODER
35
36
V reset
37
38
STV
39
40
41
42
43
44
45
FRP
CKV
46
CLOCK
FRAME
COUNTER
reset
47
MASK GENERATION
48
BACKGROUND AREA DETECTION
60
DECODER
49
F reset
VWASK
50
61
51
PTWH
PTA1S
PTAF
SPART
54
FLASH
PARTIAL
(L=NORMAL, H=PARTIAL)
52
53
65
RDATA
GDATA
BDATA
55
56
57
R_OUT
G_OUT
B_OUT

FIG. 26